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APPLICATION FOR LETTERS PATENT

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Method Of Forming A Non-Volatile Resistance  
Variable Device, And Non-Volatile Resistance  
Variable Device

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1       **Method Of Forming A Non-Volatile Resistance Variable Device, And**  
2       **Non-Volatile Resistance Variable Device**

3       **TECHNICAL FIELD**

4           This invention relates to non-volatile resistance variable devices and  
5       methods of forming the same.

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8       **BACKGROUND OF THE INVENTION**

9           Semiconductor fabrication continues to strive to make individual  
10       electronic components smaller and smaller, resulting in ever denser integrated  
11       circuitry. One type of integrated circuitry comprises memory circuitry where  
12       information is stored in the form of binary data. The circuitry can be  
13       fabricated such that the data is volatile or non-volatile. Volatile storing  
14       memory devices result in loss of data when power is interrupted. Non-  
15       volatile memory circuitry retains the stored data even when power is  
16       interrupted.

17           This invention was principally motivated in making improvements to the  
18       design and operation of memory circuitry disclosed in the Kozicki et al. U.S.  
19       Patent Nos. 5,761,115; 5,896,312; 5,914,893; and 6,084,796, which ultimately  
20       resulted from U.S. Patent Application Serial No. 08/652,706, filed on May 30,  
21       1996, disclosing what is referred to as a programmable metalization cell.  
22       Such a cell includes opposing electrodes having an insulating dielectric  
23       material received therebetween. Received within the dielectric material is a  
24       fast ion conductor material. The resistance of such material can be changed

1 between highly insulative and highly conductive states. In its normal high  
2 resistive state, to perform a write operation, a voltage potential is applied to  
3 a certain one of the electrodes, with the other of the electrode being held  
4 at zero voltage or ground. The electrode having the voltage applied thereto  
5 functions as an anode, while the electrode held at zero or ground functions  
6 as a cathode. The nature of the fast ion conductor material is such that it  
7 undergoes a chemical and structural change at a certain applied voltage.  
8 Specifically, at some suitable threshold voltage, plating of metal from metal  
9 ions within the material begins to occur on the cathode and grows or  
10 progresses through the fast ion conductor toward the other anode electrode.  
11 With such voltage continued to be applied, the process continues until a  
12 single conductive dendrite or filament extends between the electrodes,  
13 effectively interconnecting the top and bottom electrodes to electrically short  
14 them together.

15 Once this occurs, dendrite growth stops, and is retained when the  
16 voltage potentials are removed. Such can effectively result in the resistance  
17 of the mass of fast ion conductor material between electrodes dropping by a  
18 factor of 1,000. Such material can be returned to its highly resistive state  
19 by reversing the voltage potential between the anode and cathode, whereby  
20 the filament disappears. Again, the highly resistive state is maintained once  
21 the reverse voltage potentials are removed. Accordingly, such a device can,  
22 for example, function as a programmable memory cell of memory circuitry.

23 The preferred resistance variable material received between the electrodes  
24 typically and preferably comprises a chalcogenide material having metal ions

1 diffused therein. A specific example is germanium selenide with silver ions.  
2 The present method of providing the silver ions within the germanium selenide  
3 material is to initially deposit the germanium selenide glass without any silver  
4 being received therein. A thin layer of silver is thereafter deposited upon  
5 the glass, for example by physical vapor deposition or other technique. An  
6 exemplary thickness is 200 Angstroms or less. The layer of silver is  
7 irradiated, preferably with electromagnetic energy at a wavelength less than  
8 500 nanometers. The thin nature of the deposited silver enables such energy  
9 to pass through the silver to the silver/glass interface effective to break a  
10 chalcogenide bond of the chalcogenide material, thereby effecting dissolution  
11 of silver into the germanium selenide glass. The applied energy and  
12 overlying silver result in the silver migrating into the glass layer such that  
13 a homogenous distribution of silver throughout the layer is ultimately achieved.

14 It can be challenging to etch and to chemical-mechanical polish metal  
15 ion containing chalcogenide materials. Accordingly it would be desirable to  
16 develop memory cell fabrication methods which avoid one or both of etching  
17 or polishing such materials. It would also be desirable to develop alternate  
18 methods from that just described which incorporate the metal ions into  
19 chalcogenide materials. While the invention was principally motivated in  
20 achieving objectives such as these, the invention is in no way so limited.  
21 The artisan will appreciate applicability of the invention in other aspects of  
22 processing involving chalcogenide materials, with the invention only being  
23 limited by the accompanying claims as literally worded and as appropriately  
24 interpreted in accordance with the doctrine of equivalents.

## SUMMARY

The invention includes non-volatile resistance variable devices and methods of forming the same. In one implementation, a method of metal doping a chalcogenide material includes forming a metal over a substrate. A chalcogenide material is formed on the metal. Irradiating is conducted through the chalcogenide material to the metal effective to break a chalcogenide bond of the chalcogenide material at an interface of the metal and chalcogenide material and diffuse at least some of the metal outwardly into the chalcogenide material. In one implementation, a method of metal doping a chalcogenide material includes surrounding exposed outer surfaces of a projecting metal mass with chalcogenide material. Irradiating is conducted through the chalcogenide material to the projecting metal mass effective to break a chalcogenide bond of the chalcogenide material at an interface of the projecting metal mass outer surfaces and diffuse at least some of the projecting metal mass outwardly into the chalcogenide material. In certain aspects, the above implementations are incorporated in methods of forming non-volatile resistance variable devices.

In one implementation, a non-volatile resistance variable device in a highest resistance state for a given ambient temperature and pressure includes a resistance variable chalcogenide material having metal ions diffused therein. Opposing first and second electrodes are received operatively proximate the resistance variable chalcogenide material. At least one of the electrodes has a conductive projection extending into the resistance variable chalcogenide material.

## BRIEF DESCRIPTION OF THE DRAWINGS

Preferred embodiments of the invention are described below with reference to the following accompanying drawings.

Fig. 1 is a diagrammatic sectional view of a semiconductor wafer fragment in process in accordance with an aspect of the invention.

Fig. 2 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 1.

Fig. 3 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 2.

Fig. 4 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 3.

Fig. 5 is a view of the Fig. 1 wafer fragment at an alternate processing step subsequent to that shown by Fig. 3.

Fig. 6 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 4.

Fig. 7 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 6.

Fig. 8 is a view of the Fig. 1 wafer fragment at a processing step subsequent to that shown by Fig. 7.

## DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

This disclosure of the invention is submitted in furtherance of the constitutional purposes of the U.S. Patent Laws "to promote the progress of science and useful arts" (Article 1, Section 8).

Referring to Fig. 1, a semiconductor wafer fragment 10 is shown in but one preferred embodiment of a method of forming a non-volatile resistance variable device. By way of example only, example such devices include programmable metalization cells and programmable optical elements of the patents referred to above, further by way of example only, including programmable capacitance elements, programmable resistance elements, programmable antifuses of integrated circuitry and programmable memory cells of memory circuitry. The above patents are herein incorporated by reference. The invention contemplates the fabrication techniques and structure of any existing non-volatile resistance variable device, as well as yet-to-be developed such devices. In the context of this document, the term "semiconductor substrate" or "semiconductive substrate" is defined to mean any construction comprising semiconductive material, including, but not limited to, bulk semiconductive materials such as a semiconductive wafer (either alone or in assemblies comprising other materials thereon), and semiconductive material layers (either alone or in assemblies comprising other materials). The term "substrate" refers to any supporting structure, including, but not limited to, the semiconductive substrates described above. Also in the context of this document, the term "layer" encompasses both the singular and the plural unless otherwise indicated. Further, it will be appreciated by the artisan that

1 "resistance setable semiconductive material" and "resistance variable device"  
2 includes materials and devices wherein a property or properties in addition to  
3 resistance is/are also varied. For example, and by way of example only, the  
4 material's capacitance and/or inductance might also be changed in addition to  
5 resistance.

6 Semiconductor wafer fragment 10 comprises a bulk monocrystalline  
7 semiconductive material 12, for example silicon, having an insulative dielectric  
8 layer 14, for example silicon dioxide, formed thereover. A conductive  
9 electrode material 16, also termed a first metal layer, is formed over and on  
10 dielectric layer 14. By way of example only, preferred materials include any  
11 of those described in the incorporated Kozicki et al. patents referred to above  
12 in conjunction with the preferred type of device being fabricated. Layer 16  
13 might constitute a patterned electrode for the preferred non-volatile resistance  
14 variable device being fabricated. Alternately by way of example only,  
15 layer 16 might constitute a patterned line or extension of a field effect  
16 transistor gate, with a subsequently deposited layer principally serving  
17 essentially as the electrode. An example preferred material for layer 16 is  
18 elemental tungsten deposited to an exemplary thickness of from about  
19 100 Angstroms to about 1000 Angstroms. In the illustrated example, layer 16  
20 has been patterned, and another dielectric layer 17 has been deposited and  
21 planarized as shown.

22 A second metal layer 18 is formed (preferably by a blanket deposition)  
23 on first metal layer 16. An exemplary preferred material in conjunction with  
24 the non-volatile resistance variable device being fabricated is elemental silver.



1 A preferred thickness for layer 18 is from about 175 Angstroms to about 300  
2 Angstroms.

3 Referring to Fig. 2, second metal layer 18 is formed into a  
4 structure 20, and first metal layer 16 is outwardly exposed. Such is  
5 preferably conducted by subtractive patterning of metal layer 18, for example  
6 by photolithographic patterning and etch. In one implementation, structure 20  
7 can be considered as comprising a metal mass projecting from underlying  
8 substrate material and having outer surfaces comprised of a top surface 22  
9 and opposing side surfaces 24 which join with top surface 22 at respective  
10 angles. The preferred angles are preferably within about 15° of normal, with  
11 normal angles being shown in the figures.

12 Referring to Fig. 3, a chalcogenide material 26 is formed over the  
13 substrate on second metal structure 20 outer surfaces 22 and 24, and on  
14 exposed first metal layer 16. Such is preferably formed by blanket physical  
15 vapor deposition. A preferred deposition thickness for layer 26 is preferably  
16 less than three times the thickness of deposited layer 18, with an example  
17 being from about 525 Angstroms to about 900 Angstroms. More preferred  
18 is a thickness to provide layer 18 at 20% to 50% of layer 26 thickness.  
19 Exemplary preferred chalcogenide materials include those disclosed in the  
20 Kozicki et al. patents referred to above. Specific preferred examples include  
21 a chalcogenide material having metal ions diffused therein represented by the  
22 formula  $Ge_xA_y$ , where "A" is selected from the group consisting of Se, Te  
23 and S and mixtures thereof. The illustrated example provides but one  
24 possible example of surrounding the exposed outer surfaces of a projecting

1 metal mass with chalcogenide material in accordance with but one aspect of  
2 the invention.

3 Referring to Fig. 4, irradiating is conducted through chalcogenide  
4 material 26 to patterned second metal 18 effective to break a chalcogenide  
5 bond of the chalcogenide material at an interface with the patterned second  
6 metal outer surfaces and the chalcogenide material, and to diffuse at least  
7 some of second metal 18 outwardly into the chalcogenide material. Metal  
8 doped material 27 is formed thereby. Therefore as shown in the preferred  
9 embodiment, only a portion of blanket deposited chalcogenide material  
10 layer 26 is doped with second metal 18. A preferred irradiating includes  
11 exposure to actinic radiation having a wavelength below 500 nanometers, with  
12 radiation exposure at between 404 - 408 nanometers being a more specific  
13 example. A specific example in a suitable UV radiation flood exposure tool  
14 is  $4.5 \text{ mW/cm}^2$ , 15 minutes, 405 nm wavelength, at room ambient temperature  
15 and pressure.

16 In the depicted and preferred embodiment, the irradiating diffuses only  
17 some of the metal from layer 18 outwardly into chalcogenide material, leaving  
18 a remnant structure 20a. Accordingly, the projecting metal mass 20a has a  
19 shape after the irradiating which is maintained in comparison to original  
20 shape 20, but at a reduced size. Fig. 5 illustrates a lesser preferred alternate  
21 embodiment 10a whereby the irradiating and/or layer dimensions might be  
22 modified such that the irradiating diffuses all of projecting metal mass 20  
23 outwardly into the chalcogenide material.  
24

1       The preferred exemplary tungsten material of layer 16 does not  
2       appreciably diffuse into layer 26. Referring to Fig. 6 and regardless,  
3       chalcogenide material 26 not doped with metal 18 is substantially selectively  
4       etched from metal doped portion 27 of the chalcogenide material. In the  
5       context of this document, "substantially selective" means a relative etch ratio  
6       of layer 26 relative to layer 27 or at least 3:1. In the illustrated and  
7       preferred embodiment, such etching is preferably conducted to remove all of  
8       chalcogenide material 26 which has not been doped with metal 18. The  
9       preferred etching comprises dry anisotropic etching, preferably dry plasma  
10      anisotropic etching. A principle preferred component of such etching gas  
11      comprises  $\text{CF}_4$ . Additional preferred gases in the chemistry include  $\text{C}_2\text{F}_6$  and  
12       $\text{C}_4\text{F}_8$ . Top power is preferably maintained at 500 watts, with the lower  
13      wafer susceptor being allowed to float. Susceptor temperature is preferably  
14      maintained at about 25°C, and an exemplary reactor pressure is 50 mTorr.  
15      By way of example only, a specific example in a reactive ion etcher is  $\text{CF}_4$   
16      at 50 sccm, Ar at 25 sccm, susceptor temperature at 25°C, pressure of  
17      50 mTorr and top power at 500 Watts.

18       Referring to Fig. 7, an insulating layer 30 has been deposited and  
19       metal doped chalcogenide material 27 has been exposed. An example and  
20       preferred material for layer 30 is silicon nitride.

21       Referring to Fig. 8, an outer conductive electrode layer 32 has been  
22       deposited and patterned to form the outer electrode of the preferred non-  
23       volatile resistance variable device. Example materials include those disclosed  
24       in the above Kozicki et al. patents. In the illustrated and described preferred

1 example, silver structure 20a might be designed and fabricated to constitute  
2 the effective quantity of silver for programming the device with no silver  
3 being provided in electrode 32. Alternately by way of example only, layer  
4 16 might also constitute elemental silver with no silver being provided in  
5 electrode 32. Further, by way of example only, electrode 32 might  
6 principally comprise elemental silver, or at least a lower silver portion in  
7 contact with the chalcogenide material 27.

8 The above-described preferred embodiment example was in conjunction  
9 with fabrication of a non-volatile resistance variable device. However, the  
10 invention also contemplates metal doping a chalcogenide material independent  
11 of the device being fabricated, and in the context of the accompanying claims  
12 as literally worded regarding methods of metal doping a chalcogenide material.  
13 Further, the preferred example is with respect to formation of a projecting  
14 metal from an underlying substrate having chalcogenide material received  
15 thereover. However, the invention is in no way so limited and also  
16 contemplates, by way of example only, diffusing metal from an entirely flat,  
17 or other, underlying surface into overlying chalcogenide material.

18 The invention also contemplates non-volatile resistance variable devices  
19 independent of the method of manufacture. In one implementation, such a  
20 device includes a projecting metal mass (for example mass 20a) extending  
21 outwardly from a first metal layer laterally central into resistance variable  
22 chalcogenide material. In one aspect, the invention contemplates the device  
23 being in a highest resistance state for a given ambient temperature and  
24 pressure. For example, the Fig. 8 device as depicted is in such a highest

1 state of resistance. Progressively lower states of resistance for a given  
2 ambient temperature and pressure will exist as a silver dendrite, in the  
3 preferred embodiment, progressively grows from an electrode to the point of  
4 contacting the opposing electrode. Fig. 8 depicts but one exemplary  
5 embodiment of such a non-volatile resistance variable device having such a  
6 laterally central located projecting mass relative to material 27.

7 The invention also contemplates a non-volatile resistance variable device  
8 in a highest resistance state for a given ambient temperature and pressure  
9 independent of a conductive projection which is so centrally located. Such  
10 comprises a resistance variable chalcogenide material having metal ions diffused  
11 therein. Opposing first and second electrodes are received operatively  
12 proximate the resistance variable chalcogenide material, with at least one of  
13 the electrodes comprising a conductive projection extending into the resistance  
14 variable chalcogenide material. Provision of such a structure is in no way  
15 shown or suggested in a highest resistance state for a given ambient  
16 temperature and pressure in any of the teachings and drawings of the above-  
17 described Kozicki et al. patents.

18 In compliance with the statute, the invention has been described in  
19 language more or less specific as to structural and methodical features. It  
20 is to be understood, however, that the invention is not limited to the specific  
21 features shown and described, since the means herein disclosed comprise  
22 preferred forms of putting the invention into effect. The invention is,  
23 therefore, claimed in any of its forms or modifications within the proper  
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1 scope of the appended claims appropriately interpreted in accordance with the  
2 doctrine of equivalents.  
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